HIGH level.

A2 cont'd

9. (Once Amended) The MOSFET logic circuit as in claim 1, wherein a delay of the MOSFET logic circuit is one of a delay of a transmission gate formed by first and second transistors of the three transistors, and a delay of a third transistor of the three transistors.

REMARKS

Reconsideration of the application is respectfully requested.

In the Office Action dated March 29, 2002, Claims 1-9 were objected to for not including the word "MOSFET". Claims 1-2 and 4-9 are amended to include "MOSFET" in describing the logic circuit. Claim 4 was further objected to because of clerical error. Line 4 of claim 4 is amended to recite "the first transistor." These amendments are believed to overcome the objections raised.

Also in the Office Action, Claims 1-9 were rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 5,528,177 ("Sridhar et al."). In this Reply, Claim 1 is amended to recite that first and second transistors of the three transistors form a transmission gate outputting one signal, wherein at least two input signals are provided to the first and second transistors and an output signal indicative of an OR operation performed on first and second input signal of the at least two input signals is output from the MOSFET logic circuit.

It is submitted that Sridhar et al. does not disclose or suggest every element claimed in Claim 1. For example, Fig. 2g of Sridhar et al. does not disclose or suggest first and second transistors of three transistors that form a transmission gate outputting one signal, wherein two input signals are provided to the first and second transistors and an output signal indicative of an OR operation performed on the two input signals is output from the MOSFET logic circuit.

Instead, Fig. 2g of Sridhar et al. appears to disclose a pair of CFET logic circuits for performing NOR and OR functions. Sridhar et al. appears to require the pair for performing an OR function, each one CFET logic circuit receiving an input signal. Sridhar et al. does not disclose two inputs to two transistors forming a transmission gate, wherein an output indicative of OR signal of the two inputs is output as claimed in Claim 1. Accordingly, it is submitted that Claim1 is patentable over the cited reference.

Claims 2, 4-9 are dependent claims of Claim 1, and therefore, for at least the same foregoing reasons, it is submitted that these claims are patentable over the cited references.

Attached is a marked-up version of the changes made to the claims by the current amendment according to 37 C.F. R. §1.121. The attached page is captioned "Version with Markings to Show Changes Made."

Applicants believe that Claims 1-2, 4-9 are now in condition for allowance. If the Examiner has any questions regarding this communication or feels that an interview would be helpful in advancing the prosecution of this application, the Examiner is requested to contact Applicants' undersigned attorney.

Respectfully submitted,

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Version with Markings to Show Changes Made

IN THE CLAIMS:

Please amend Claims 1-2, 4-9 as follows and cancel Claim 3.

1. (Once Amended) A MOSFET logic circuit for performing a logic OR operation comprising three transistors, first and second transistors of the three transistors forming a transmission gate outputting one signal, and wherein at least two input signals are provided to the [circuit] the first and second transistors and an output signal indicative of an OR operation performed on a first and second input signal of the at least two input signals is output from the MOSFET logic circuit.

2. (Once Amended) The MOSFET logic circuit as in claim 1, wherein the three transistors include first and second PMOS transistors and one NMOS transistor.

4. (Once Amended) The MOSFET logic circuit as in claim 1, wherein the first input signal is provided to a source of first and second transistors of the three transistors, the second input signal is provided to a gate of the second transistor, and a complement of the second input signal is provided to a gate of the [second] first transistor.

5. (Once Amended) The MOSFET logic circuit as in claim [3] 1, wherein a complement of the second input is provided to a gate of a third transistor of the three transistors.

6. (Once Amended) The MOSFET logic circuit as in claim 1, wherein the at least two input signals to the [circuit] first and second transistors further comprise a complement of the second input signal.

7. (Once Amended) The MOSFET logic circuit as in claim [3] 1, wherein when the second input signal has a logic LOW level the output of the MOSFET logic circuit is an output signal of the transmission gate.

8. (Once Amended) The MOSFET logic circuit as in claim [3] 1, wherein a third transistor of the three transistors is a pull-up transistor, and when the second input signal has a logic HIGH level the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor, which pulls up the output signal from the transmission gate to a logic HIGH level.

9. (Once Amended) The MOSFET logic circuit as in claim 1, wherein a delay of the MOSFET logic circuit is one of a delay of a transmission gate formed by first and second transistors of the three transistors, and a delay of a third transistor of the three transistors.